This Notes makes First Edition obsolete and consists of two parts:

Part 1  Previous First Edition .... pp.1-31

Part 2  Mainly applicable to JP-8 units with Serial Numbers 171700 and above .... pp.32-46

Parts List Change .... p.47

Appendix ......... pp.48-50

BEFORE READING
PLEASE CHECK FOR CHANGE INFORMATION AND CONTENTS AT PAGES 32 AND 33 OF THIS NOTES.

SPECIFICATIONS

Keyboard: 61 Note, 5 Octaves
VCO: VCO-2 Fine Tune Range: +50 Cents
VCF: Slope: 12-Octave, 24-Octave
ENV: Key Follow: 0 - 100%
ENV-L: Attack Time: 1ms - 5s
LFO: Decay Time: 1ms - 10s
Rate: 0.05 - 40Hz
Delay Time: 1ms - 10s
Master Tune Range: ±50Hz

Arpeggio:
Rate: 1 - 20Hz
Audio Outputs
Upper:
VCF: 0dBm, 600 Ohm, Balanced
ENV: Off, 600 Ohm, Balanced
Sustain Level: 0 - 100%

VCO-2: +20dBm, 1kHz, Unbalanced
VCF: 0dBm/—20dBm, 1kHz, Unbalanced
Lower:
VCF: 0dBm, 600 Ohm, Balanced
VCO-2: 0dBm/—20dBm, 1kHz, Unbalanced
Gate:
VCF: Off - 0V, On - +15V
Sustain Level: 0-100%

Dimensions:
Keyboard (complete) SK-361C (004H008)

Power Consumption:
90W

JP-8 PANEL PARTS LIST

1. Pot. GM70R-K20B54 (50KB x 2) (13219812)
2. Pot. GM70R-K20AC54 (50KA, C) (13219811)
3. Pot. LFE9R-C16A55 (500KA) (13339414)
4. Switch SRM1034-K15 (13119301)
5. Switch SLE622-18P.S (13139137)
6. Pot. VM10R-K20BN14 (10KB) (13129725)
7. Pot. LFE9R-C16BN14 (10KB) (13339415)
8. Switch SQPR-24-12P (13169503)
9. Pot. LFE9R-C16BN54 (50KB) (13339413)
10. Pot. MF9R-C16BN54 (50KB x 2) (13159302)
11. Pot. VM10R-K20A55 (50KA) (13119231)
12. Pot. VM10R-K20BC54 (50KC) (13129723)
13. Switch SLE622-18P (13139135)
14. Switch w/key top KEH10003 (13129717)
15. Bled assy PB-4 (029-022)
16. Cover LED L525RA (15029404)
17. Switch KH11901 (13169601)

Buttons
No.1, 3B RED (016H018)
No.2, No.3-37 ORANGE (016H012)
No.6-9, No.30-33 YELLOW (016H017)
No.10-13, No.21-28 WHITE (016H010)
No.14, 15, 29 GREEN (016H014)
No.16-18, No.39-41 BLUE (016H013)
No.19, 20 DARK BLUE (016H011)

18. Pot. VM10A-K15BS54 (50KB CT) (13229131)
19. Switch SLE622-18P (13139136)

Printed in Japan BB-2
DISASSEMBLY
Remove screws ①, ②, and ③.

NOTE:
Preparation of a stay and a prop is recommended for a stable top panel rest.

PRECAUTIONS
1. Do not pinch flat cables in the PCBs when closing panel assemblies. Prongs on PCBs will pierce humped cable, causing circuits to malfunction. Stretch rolling cable out.
2. Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, PCBs are temperature-sensitive.
### WIRING DATA TABLE

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**CPU BOARD**

- H1: 2VDC
- I: 2VDC
- M: 2VDC
- H: 2VDC
- GND: 2VDC

- 1: VCO E-1
- 2: E-2
- 3: GND
- 4: VCO F-1
- 5: E-2
- 6: GND
- 7: VCO G-1
- 8: G-2
- 9: GND
- 10: VCO H-1
- 11: H-2
- 12: GND

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MODULE BOARD BLOCK DIAGRAM

MODULE BOARD BLOCK DIAGRAM

DESTINATION
MODULE BOARD.

PANEL BOARD BLOCK DIAGRAM
CPU BOARD BLOCK DIAGRAM

MOD-CON BOARD BLOCK DIAGRAM
ALL ARROWS HAVING NO DESTINATION IDENTIFIER CONNECT TO MODULE BOARD.

INTERFACE BOARD BLOCK DIAGRAM
Refer to Page 38 for:

CPU CHANGE INFORMATION

CAUTIONS ON MODULE CONTROLLER BOARD REPLACEMENT
RAM (MOD CON BOARD) REPLACEMENT

CPU BOARD WILL BE AFFECTED BY THESE REPLACEMENTS
MODULE CONTROLLER

OPH123(149H123) (pcb 052H269)

SN 090600-192099

REFER TO PAGES
49-50 for SN up to 090699
36-37 for SN 202100-up
37-38 for PCB or RAM REPLACEMENT
There are two different GND lines. "^" is not connected to "^" on the PCB.

Hi-Freq. Ref. (on +10.6k, T250, IC108), GND, R273, VR230.
MODULE BOARD
OPH124(149H124)
 pcb 052H270

SEE PAGE 48
For SN up to 090599

- 425G
- Selected on slow rate
- Tlocale 8 processor
- CR2 SR
- Cramon, 425
- Crfegdeath, 425
- Metal films 425
- PA7700043050661
- Polarity: SP102
- 2S11W1-9R
- 2S0815-9R
- 2S07121-9R
- 2SK190-9R
- 2SK110-9R
- 2SK11-9R
- NP110
- 152-73
- 3A62
- 87-6P

- A or B
- selected on UF (gpm)
- replacement should be
- if the existing

- Selected on offset
- per units data

- 5RF
- Test point LO-28 (TRI-GEN)
- Poly styrene film
- Bi-polar
See pp. 34–35 for SN171700 and up

CAUTION
When replacing Interface board bearing edition no. 052H26B (and below) with PC8 of 052H26B (and above), refer to pp. 34 and 35 for PROMs versions of CPU board.
PANEL BOARD A  OPH125(149H125) (pcb 052H271)

Component side

Foil side
ADJUSTMENTS

DISASSEMBLY
Follow procedure on page 2. Preparation of a STAY (chain or string) and prop is advisable for a stable top panel rest.

PRECAUTIONS
Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, most circuits are temperature-sensitive.
The adjustments on the JP-8 should not be done more than necessary. Adjustments merely attempted on a particular module (VOICE) might cause sound balance away from entire VOICEs and can, in an extreme case, require the same procedures to be done fifteen times for the remainder.

DESIGNATION - TEST POINT, TRIMMER, PCB -
For PCBs that are identical in circuit configuration, most adjustment steps, test points and trimmers do not refer to a particular PCB or module (VOICE), they may be read as ones on a PCB to be adjusted.

TEST MODES
Adjustments on the JP-8 proceed in TEST MODEs. Although three TEST MODEs are available for the adjustments, TEST MODE (3) is chosen in this manual unless otherwise specified. (For more details refer to TEST MODE in Circuit Description - separate copy.)

TEST MODE
SW-1, LED switch, in close position, allows LEDs (TEST LED) located right to it to be energized regardless of MODE (NORMAL or TEST) when gate signals are fed to them individually. The LEDs function as assignment indicator just as Patch Number LEDs do. Test LEDs find extended application for learning and checking the assignments varying to MODEs (KEY, PANEL and ASSIGN) in Normal mode.
Patch Number LEDs are lit automatically in sequence immediately after TUNE is touched, representing module A VCO-1 (leftmost LED), A VCO-2 (No. 2 LED) and so on; the first cycle for Upper modules' and the second for Lower. Their lighting period is proportional to degree of VCO detune from standard pitches. An LED staying on and won't pass illumination to the next one claims checking of its mated VCO having been far out of computer controllable range.
TEST MODEs 2 and 3 are identical to each other in function, but any panel disassembly is required for mode 2 if the purpose is only to check Key Assignment or VCO detune.

FOR SATISFACTORY SERVICE WORK
1. Dump user's preset memory on tape before attempting adjustments and troubleshooting.
2. If TUNE was pressed in previous adjustments, be sure to power off and on the JP-8 before making adjustment which must be done without computer-tune.
3. Plural keying and miskeying will disorder key assignment sequence. Push HOLD or ASSIGN MODE to off and again to on, as appropriate, to restore the order.
Use monitor amp to detect erroneous key assignmanet that LED does not distinguish.
4. Make a practice of pushing MANUAL after changing PANEL MODEs.
5. Restore SW-1-1 and SW-1-2 to OPEN and load back the data on tape before return the unit to the customer.
12. VCO LEVEL

MODULE (MOD)

IB Roland

JUPITER

See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4.
2. Press A2 key, adjust VR13 for 10V p-p reading.

13. VCF KEY FOLLOWER

MODULE (MOD) MODULE CONTROLLER (MOD CON)

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166 lead.
3. Turn MOD VR14 fully clockwise. The VCFs resonate. VR14 and VR20 will be readjusted in later para.
4. Press C2 key, adjust scope timebase and VCF FREQ to display one complete cycle. (across the graticules, same for the rest para.) MOD VR20 may be used for fine adjustment.

Steps 2 and 3 interact, repeat steps as required.

14. VCF WIDTH

MODULE (MOD) MODULE CONTROLLER (MOD CON)

Para. 13-17 must be performed in sequence.

1. With scope to MOD TP-6 set timebase to 1ms (2ms)/div.
2. Press C2 key, adjust VCF ENV MOD and MOD VR20 to display one complete cycle.

On JP-8's S/N **0600 and subsequent, read figures in parenthesis.

2. Set CO FREQ to 10, scope timebase to 5us/div (20us/div), Adjust VR19 to display one complete cycle (5 cycles).

Steps 2 and 3 interact, repeat steps as required.

15. VCF ENV MOD

MODULE (MOD) MODULE CONTROLLER (MOD CON)

Para. 13-17 must be performed in sequence.

1. Press C2 key, adjust CO FREQ and MOD VR20 to display exactly one complete cycle.
2. Reset VCF ENV MOD to 10, timebase to 50us/div. Adjust VR21 to display 16 complete cycles.

16. VCF TUNE

MODULE (MOD) MODULE CONTROLLER (MOD CON)

Para. 13-17 must be performed in sequence.

Change setup in para. 15 step 2: ENV MODE to 0; CO FREQ to 5 (S/N **0600 — 4); scope to MOD TP-6 with A-442 reference fed to H IN.

1. Press A2 key, adjust VR20 for 1:1 Lissajous.

17. RESONANCE LEVEL

MODULE (MOD)

Para. 13-17 must be performed in sequence.

Change setup in para. 16: SOURCE MIX to VCO-1; CO FREQ to 10; Scope to INT TRIG.

1. Press A2 key (S/N **0600 — E3 key), adjust VR14 for the figure.
18. VCA LEVEL

MODULE (MOD) MODULE CONTROLLER (CON) (early JP-8)

- See appendices for adjustment locations and glossary.
- Although CON VR5 is included in part 1, the trimpot is replaced by 10k resistor on later products.
- When adjusting MOD replacement, ignore VR5 trimming, following Part 2.
- Connect scope to TP-6 or R166 lead.

PART 1
1. Set MOD VR18 wiper to midpoint.

PART 2

19. VCA BALANCE

MODULE (MOD) MODULE CONTROLLER (CON)

- See appendices for adjustment locations and glossary.
- 1. Place ground to CON TP-4 or D20 cathode.
- 2. Connect scope to MOD TP-6 or R166. Switch scope to Decoupling, vertical range to 20mV/div.
- 3. While tapping a key, adjust VR17 so that DC variations are minimized.

20. ENVELOPE TOTAL TIME

MODULE (MOD)

- See appendices for adjustment locations and glossary.
- This adjustment proceeds on the assumption that all VOICES' ENVs are unadjusted. When adjusting particular module, start from step 3 with scope V IN connected to TP-6 of well calibrated module.

ENV-1
1. Connect scope to MOD GH R183B lead or TP-8B.
2. While holding a key, time Attack period on scope. Adjust MOD H VR22 for 6-sec attack period.
4. Press and hold a key repeatedly, adjust both ENV-1 ATTACK (around 4-5) and timebase VARI or vernier so that envelope's falling edge is centered on the screen.
5. Shift V lead to TP-8 of the module to be adjusted. Adjust the VR22 for centered falling edge.

ENV-2
The procedure is similar to those in ENV-1, but connect scope to R189 lead or TP-7 and adjust ENV-2 ATTACK and VR23.
7. ENV-1 S OFFSET
MODULE CONTROLLER (CON)
Applicable to the PCB equipped with VR9

1. Connect scope to CON TP-7.
2. Set scope V to 20mV/div.
3. Adjust CON VR9 for 0V reading.

7. VCO ENV MOD BAL
MODULE (MOD)
On JP-8 mounting CON with VR9, this adjustment must follow para. 7-1.

1. Connect scope to MOD TP-4 with A-442 reference to H IN.
2. Adjust MOD VR8 for still Lissajous. (Frequency is same as in step 3.)

8. VCO ENV MOD DEPTH
MODULE (MOD)
This adjustment must follow para. 7. See appendices for adjustment locations and glossary.

1. Press A0 key, adjust MASTER TUNE so that Lissajous is 1:1.
2. Switch VCO-2 WAVE to square; VCO-1 to 16’. Adjust MOD VR11 to display Lissajous observed in step 1.

9. VCO CROSS MOD BALANCE (X-MOD)
MODULE (MOD) MODULE CONTROLLER (CON)

1. Connect scope to MOD TP-4 or R130 lead. Trigger on the negative edge (positive S/N **0600).
2. Press C2 key, adjust MOD VR12 for 30ps space width.

NOTE:
VR12’s interact to each other. Check other voices for mark/space ratio. Readjust as necessary.
BEFORE STARTING ADJUSTMENTS
ALLOW AT LEAST 30 MINUTES FOR WARUP PERIOD

1. DC SUPPLY
POWER SUPPLY BOARD

1. Connect Digital voltmeter (DVM) to
-15V (terminal 9, 10, 11).
2. Adjust VR1 for
-15V±10mV reading.
3. +15V should be
+15V±50mV.
4. +5V should be
5V±400mV.

2. DC SUPPLY (VCO)
MODULE CONTROLLER
See appendices for adjustment locations and glossary.
MODS A, B, C and D
1. Connect DVM to MOD AB IC1 pin 4 (—'VOD).
2. Adjust upper CON VR4 for -13V±5mV.
3. IC1 pin B should read +13V±200mV.

MODS E, F, G and H
1. Disconnect flatcables at upper CON LM1 and HL.
Observe the note in CON Layout, appendix.
2. Perform step 1-3 above for lower PCBs.

3. PANEL POTs VOLTAGES
INTERFACE (INT) PANEL BOARD A
See appendices for locations and glossary.
1. Connect DVM to INT TP-3 or R83 (10k) lead facing outside. (See Fig. below right.)
2. Depress MANUAL.
3. Turn all the pots on the panel illustrated fully cw,
or to 10. Incomplete settings result in a fluctuating reading or dips on a screen if observed with scope.
4. Set VR1 (Panel board A) for +5V±2mV.

4. DAC
INTERFACE (INT)
See appendix for glossary.
1. Connect DVM to OUTPUT CV jack.
2. Press KEY MODE WHOLE.
3. Press C5 key, adjust VR1 for 5.000V reading.
4. Check C0-C5 keys for scaling, that those voltages are 1 V/oct increments ±2mV.

5. VCO MOD BAL
MODULE (MOD)

1. Connect DVM to MOD TP-3 or R103 lead.
2. Adjust MOD VR7 for 0.000V reading.

6. VCO TUNE
MODULE (MOD)
See appendices for adjustment locations and glossary.

Computer-tuned VCO needs to be recalibrated only if it or associated components have been replaced. If a VCO is excessively out of tune right after computer-tune, first check MOD BAL, para. 5 and KCV OUT (INT terminals IM-1, IM-3, etc.) for voltage. Second, isolate possible causes before attempting VCO adjustments.

As usual with tuning, several instruments may be used for determining frequency. The calibration proceeds by Lissajous figures with A-442 reference fed to scope's horizontal input.

1. Connect scope to MOD TP-4 or R130 lead.
2. Turn SOURCE MIX fully to VCO-1 or 2 accordingly.
3. Press A3 key, adjust trimpot T for 6064Hz.
4. Press A1 key, adjust trimpot W for 221Hz.
5. Repeat steps 3-4 until waveforms are stationary on both keys.
6. With RANGE set in '2', press A3 key and adjust L for 221Hz.
7. These trims interact to each other, repeat steps 3-6 until three notes are on the right frequency.
1. Connect scope to MOD TP-4.
   CAUTION: On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.
2. Press A2 key, adjust VR13 for 10V p-p reading.
4. Press C4 key, adjust VR16 to display 4 complete cycles.

NOTE: VR14 and VR20 will be readjusted in later para.

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166 lead.
3. Turn MOD VR14 fully clockwise. The VCFs resonate.
   Change para. 14 setup: VCF ENV MOD to 0, scope timebase to 0.2ms/div.
   1. Press C2 key, adjust CO FREQ and MOD VR20 to display exactly one complete cycle.
   2. Reset VCF ENV MOD to 10, timebase to 50μs/div.

 Adjust VR21 to display 16 complete cycles.

15. VCF ENV MDD
MODULE (MOD)   MODULE CONTROLLER (MOD CON)
Para. 13-17 must be performed in sequence.
Change setup in para. 14 step 2: ENV MODE to 0; CO FREQ to 5 (S/N **0600 — 4); scope to MOD TP-6 with A-442 reference fed to H IN.
1. Press A key, adjust VR20 for 1:1 Lissajous.

17. RESONANCE LEVEL
MODULE (MOD)
Para. 13-17 must be performed in sequence.
Change setup in para. 16: SOURCE MIX to VCO-1; CO FREQ to 10; Scope to INT TRIG.
1. Press A2 key (S/N **0600 — E3 key), adjust VR14 for the figure.
18. VCA LEVEL

PART 1
1. Set MOD V R18 wiper to midpoint.

PART 2

19. VCA BALANCE

PART 1
1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166. Switch scope to DC coupling, vertical range to 20mV/div.
3. While tapping a key, adjust VR17 so that DC variations are minimized.

20. ENVELOPE TOTAL TIME

PART 1
1. Connect scope to MOD GH R183B lead or TP-8B.
2. While holding a key, time Attack period on scope. Adjust MOD H VR22 for 6-sec attack period.
4. Press and hold a key repeatedly, adjust both ENV-1 ATTACK (around 4.5) and timebase VAR I or vernier so that envelope's falling edge is centered on the screen.
5. Shift V lead to TP-8 of the module to be adjusted. Adjust the VR22 for centered falling edge.

ENV-1
This adjustment proceeds on the assumption that all VOICES' ENVs are unadjusted. When adjusting particular module, start from step 3 with scope V IN connected to TP-8 of well calibrated module.

ENV-2
The procedure is similar to those in ENV-1, but connect scope to R189 lead or TP-7 and adjust ENV-2 ATTACK and VR23.
21. LFO MODULATION

MODULE (MOD) MODULE CONTROLLER (CON)

JUPITER-8

See appendices for adjustment locations and glossary.
1. Connect scope to CON TP-5 or RS9 lead. Set timebase to 10ms/div.
2. Adjust CON VR3 to display exactly 3 complete cycles on the scope.
3. Adjust CON VR2 for slope straightness as shown in Fig. right.
4. Shift scope to TP-4 of (Upper — MOD A; Lower — MOD E). Repeatedly holding a key, adjust CON VR8 so that VCO becomes being modulated approx. 4 sec after the key first depressed.

22. VCO LFO MODULATION

MODULE (MOD) MODULE CONTROLLER (CON)

JUPITER-8

See appendices for adjustment locations and glossary.
1. Connect scope (with A-442 into H IN) to TP-4 of (Upper — MOD A; Lower — MOD E).
2. Press A2 key, adjust MASTER TUNE for 1:1 Lissajous.
3. Set VCO LFO MOD to 10. Lissajous ratio is now changing up and down in sympathy with LFO rate. Adjust CON VR6 so that Lissajous becomes 2:1 at the highest pitch. Note that LFO modulated VCO swing equals 2 oct's.

23. VCF LFO MOD LEVEL

MODULE CONTROLLER (CON)

See appendices for adjustment locations and glossary.
1. Connect scope to TP-6 of (Upper — MOD A; Lower — MOD E).
2. Press C2 key (S/N **0600— C4 key), adjust CON VR7 for 50 percentage modulation.
3. Switch RANGE to LOW FREQ, check peaks for clip.

24. NOISE

MODULE CONTROLLER (CON)

See appendices for adjustment locations and glossary.
1. Switch VCO-2 RANGE to NORMAL. Connect scope to CON TP-4.
2. Adjust CON VR1 so that dense signal peaks are approx. SV p-p.
3. Switch RANGE to LOW FREQ, check peaks for clip.

25. BENDER OFFSET

BENDER MODULE (MOD)

See appendices for adjustment locations and glossary.
1. Connect scope to TP-4 of (Upper — MOD A; Lower — MOD E) with A-442 reference to H IN.
2. Press A2 key, adjust MASTER TUNE for stationary Lissajous.
3. Set VCO MOD switch to on, adjust VR1 (Upper) or VR2 (Lower) for stationary Lissajous.

NOTE: On JP-8 S/N **0700—, next comes para. 25-1, BENDER LEVEL.

25-1. BENDER LEVEL

BENDER MODULE (MOD)

APPLICABLE S/N with **0700 and SUBSEQUENT

1. Connect scope to TP-4 of any MOD. Press A2 key, adjust timebase and vernier (VARI) to display one complete cycle.
2. Press A3 key. Sway and hold BENDER Lever at extreme left, adjust VCO BEND to display 1 cycle.
3. Press A1 key. Sway and hold BENDER at extreme right, set VR3 for complete 1 cycle.

See appendices for glossary.
1. Join TAPE MEMORY LOAD and DUMP jacks via cable.
2. Connect scope to CPU TP-7.
3. Push VERIFY. Be sure that the JP-8 is in test mode, this is displayed in PATCH NUMBER window as —1—1—I—I, then set CPU VR1 for 50% duty cycle.
4. Push VERIFY again at the end of adjustment.

26. FSK

CPU

See appendices for glossary.
1. Join TAPE MEMORY LOAD and DUMP jacks via cable.
2. Connect scope to CPU TP-7.
3. Push VERIFY. Be sure that the JP-8 is in test mode, this is displayed in PATCH NUMBER window as —1—1—I—I, then set CPU VR1 for 50% duty cycle.
4. Press A1 key. Sway and hold BENDER at extreme right, set VR3 for complete 1 cycle.
APPENDIX I

CIRCLED NUMBERS AROUND PCB LAYOUT CORRESPOND TO PARAGRAPH NUMBERS

MODULE CONTROLLER BOARD

For accessing to MODs E, F, G, and lower MOD CON,CN connectors L1 and HL on upper MOD CON may be disconnected during service. Do not remove screws at hinges on upper PCBs for mere adjustments of lower PCBs. Remounting is not easy. Before reconnecting, switch power off. Incorrect pin connections cause short circuit ICs.

APPENDIX II

MODULE BOARD

GLOSSARY

DVM Digital Voltmeter
SCOPE Oscilloscope
CPU CPU Board
MOD Module Board
MOD Module (VOICE)
CON Module Controller Board
INT Interface Board

CIRCLED NUMBERS AROUND PCB LAYOUT CORRESPOND TO PARAGRAPH NUMBERS

On early PCBs, legends for VR13, 14, 15, 16 are incorrect. Follow this arrangement.
## PARTS LIST

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
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<tbody>
<tr>
<td>072H080</td>
<td>Panel H80 (right end block)</td>
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<td>064H100</td>
<td>Holder H100</td>
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<td>064H055B</td>
<td>Holder H55B (pot-pcb)</td>
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<td>Plate (side panel) H40 (right)</td>
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<td>Panel board GOPH 131</td>
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<td>146H062</td>
<td>POWER SUPPLY board B (220/240) PSH062</td>
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<td>POWER SUPPLY board CPSH060</td>
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<td>* TC4052BP Dual 4-channel multiplexer</td>
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### NOTATIONS

- **PCB**: Printed circuit board
- **SMD**: Surface Mount Device
- **SMD**: Surface Mount Device
- **R**: Resistor
- **C**: Capacitor
- **L**: Inductor
- **M**: Transformer
- **Q**: Diode
- **J**: Junction
- **G**: Gate
- **U**: Upper
- **D**: Down
- **P**: Power
- **S**: Signal
- **N**: Neutral
- **L**: Line
- **GND**: Ground

### KEYBOARD PARTS

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<td>13439106</td>
<td>Flat cable HI 25</td>
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### OTHERS

- **NOISE FILTER**: Filter out high-frequency signals

### SEE PP. 40 AND 47

For Parts Change Information
The following pages cover the information of Engineering changes and various aspects of JP-8 affected by the changes.

DESIGN CHANGES THAT CHANGE FEATURE OF THE JP-8

DAC
To have JP-8 more stable in pitch, DAC for KCVs is changed from 12-bit to 14-bit version.

KEY SPLIT POINT
To make JP-8 more convenient for the user to play on, key split point becomes under the control of the player.

DIGITAL COMMUNICATION INTERFACE OC-8 & DCB
To have JP-8 externally controlled through Digital Data Bus connecting either to digitally operating "musical instrument" or to Analog/Digital Interface Unit (e.g. OP-8 that accepts analog CVs in parallel), Digital Communication Interface Board (DCIB) is built in.

OC-8: First, DCIB is named OC-8 and sold as an optional kit.
DCB: Second, another version of DCIB, called DCB is incorporated in the later JP-8 as a standard feature.

The above-mentioned changes and other significant changes not found on the First Edition of JP-8 Service Notes are listed on the table right.

PARTS LIST CHANGE

APPENDIX

PCB LAYOUTS FOR EARLY 500 JP-8's
MODULE BOARD
MODULE CONTROLLER BOARD
Not published previously, these drawings will help to trace signal paths on old PCBs.
**HOW TO IDENTIFY PROM VERSION**

**CPU BOARD**

Version is indicated by hand written number or marking on the label as shown below.

Version can be displayed in PATCH NUMBER window (LOWER). Turn the JP-8 on while pressing PATCH NUMBER buttons 1 and 3.

**NOTES:**

- In 0.7 or 1.0 version, displayed number will change quickly from 07 (10) to 13.
- In 3.2 (A, B, C) and 3.3D (3.4) arrangement, number 33 (34) will change to 32 if PROM D is removed.

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<td>2.1D</td>
<td>DIGITAL COMMUNICATION INTERFACE</td>
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<td>14-BIT DAC</td>
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<tr>
<td>3.3D (3.4D)</td>
<td>DIGITAL COMMUNICATION INTERFACE</td>
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</table>

1) This is a special version. Replace each with the same one, or replace all four with a set of 3.2 and 3.4D version.
2) Co-operates with 3.3D or 3.4D for Digital Communication Interface.

**PROM REPLACEMENT**

When replacing PROMs A, B and C with different version, replace them in a set.

Version 3.2 can replace 3.1, 1.0 and 0.7
Version 3.1 can replace 1.0 and 0.7
The reverse does not hold true.
ROM 3.4 can replace 3.3D and vice versa.

**NOTES:**

- PROM D is required only when OC-8 or DCB BOARD is present.
- PROM D must be used together with A, B, C of 3.2 version and up.
- PROM D contains diagnostic programs.

Refer to P.46 for test procedure.
Difference between 3.3D and 3.4D is that the latter has debugged diagnostic program.

When need arises to modify the JP-8 or to replace parts:
First consult the table below, then refer to the right as necessary.

### INTERFACE BOARD

- p. 34

### MODULE CONTROLLER BOARD

- pp. 37, 38

### RAM IC49 of MOD CON BOARD

- p. 38

### CPU BOARD (in relation to RAM IC 49)

- p. 38

### OC-8

- OP-8 (OC-8) Service Notes

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<table>
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<tr>
<th>SERIAL NUMBER</th>
<th>PROM VERSION</th>
<th>DISPLAY</th>
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<th>FEATURES OF THE JP-8</th>
<th>ADDABLE NEW FEATURE</th>
<th>PROM VERSION</th>
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<td>OC8 built in</td>
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<td>KEY SPLIT POINT Variable</td>
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When new feature is required, replace existing part(s) with the one indicated by *.

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When new feature is required, replace existing part(s) with the one indicated by *.
INTERFACE BOARD OPH122A
(149H122A) (pcb 052H268)
SN 171700 and higher

MAJOR CHANGES

D/A CONVERTER .......... 14BIT
KEY SPLIT POINT .......... PROGRAMMABLE

This board can replace 12-bit INTERFACE BOARD when PROMs of CPU board are of correct version. See right below.

Besides suffix (A, B, etc.), the PCBs occasionally bear marks "*" and/or "o" above its code number to show the edition.
- stands for 1, and O for 5.
Example: O — 8th edition

The D/A Converter IC14 is changed from 12-bit Am6012 to 14-bit ITS80141 with this PCB version. Along with the change the following parts are also changed.

<table>
<thead>
<tr>
<th>PART</th>
<th>From</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latch</td>
<td>LS273 (TTL, IC13)</td>
<td>40H273 (CMOS, IC15)</td>
</tr>
<tr>
<td></td>
<td>LS175 (TTL, IC15)</td>
<td>40H174 (CMOS, IC13)</td>
</tr>
<tr>
<td>Multiplexer</td>
<td>LS175 (TTL, IC11)</td>
<td>40H175 (CMOS)</td>
</tr>
<tr>
<td>Multiplexer</td>
<td>4051 (IC25, IC26)</td>
<td>HD14051 (Hitachi only)</td>
</tr>
<tr>
<td>Flip-flop</td>
<td>74LS74 (IC9)</td>
<td>TC4013</td>
</tr>
<tr>
<td></td>
<td>(SN212330-UP TC40H74)</td>
<td></td>
</tr>
<tr>
<td>Gate</td>
<td>LS02 (IC22)</td>
<td>TC4001</td>
</tr>
</tbody>
</table>

Prepare PROMs for CPU board:
A, B, C
3.1 version
or 3.2 version (inevitable when OC-8 exists)
for IC34-IC38
D (when OC-8 is built in)
3.3 or 3.4 version for IC33
Replace existing PROMs with these PROMs.
Adjust DAC circuit, referring to "4. DAC" on p.25 of this book.

SUBSTITUTING THIS BOARD FOR 12-BIT DAC BOARD

Prepare PROMs for CPU board:
A, B, C
3.1 version
or 3.2 version (inevitable when OC-8 exists)
for IC34-IC38
D (when OC-8 is built in)
3.3 or 3.4 version for IC33
Replace existing PROMs with these PROMs.
Adjust DAC circuit, referring to "4. DAC" on p.25 of this book.

NOTES:
This interchange does not affect adjustment procedures except that the letter "PLL" are displayed in PATCH NUMBER window after — I — I — I during FSK adjustment steps.
At the end of Computune cycle(s), defective VCO that has not "tuned-in" is indicated in MANUAL and PATCH- NUMBER or PRESET buttons.
See p.39 for indicators and difference in computuning between 12-bit and 14-bit systems.
GUIDES ON REPLACEMENT

MODULE CONTROLLER BOARD

(For early 500 units, see p.48)

When replacing OPH123 with OPH123A, be sure to proceed the following.

Check IC49 on both PCBs (being replaced and replacement) for name. If 2101 is on the existing PCB and 5101 on the replacement, take the modification illustrated below.

When replacing Upper board or Lower only:
Adjust VR1 (NOISE LEVEL) of unchanged MOD CON board to match the noise level of new board which omits the adjustment. Reconnect R21 of unchanged MOD CON, referring to drawing to the right. This will eliminate possible loudness differences between U and L voices.

IC49 OF MOD CON BOARD (MODIFICATION ON CPU BOARD)

(RAMs 2101 and 5101)

Below, two minor modifications (independent of RAM change) are also indicated:
Reconnection of IC37 and addition of 10UF at IC30 pin 8

Insertion of 5101 into a place previously occupied by 2101 requires pin 5 of IC23 on CPU board to be grounded. This reconnection as illustrated is to protect the data on panel control from garbled—while a control is being reset, some of other controls are also detected as moving; in extreme case no voice would sound. This is due to the fact that two RAMs differently respond to the same timing signal.
This modification has no adverse effect on 2101.
IMPORTANT
When replacing MOD CON BOARD or RAM IC49,
SEE PAGE 38 (P.48 for early 500 units).

CHANGE INFORMATION

(Each heading is followed by address to the circuit diagram.)

1. NOISE GENERATOR (D-H, 18-27)
   IC3: from TL082 to BA662 having AGC.
   NOISE LEVEL VR1: omitted

2. SAMPLING SIGNAL
   Previous circuit: Only white noise is routed to S/H circuit regardless of VCO-2 RANGE position.
   New circuit: Pink noise is selected for S/H when RANGE is in LOW position.

3. D/A CONVERTER (O-R, 23)
   Ladder Resistors: from discrete to resistor array

4. NOISE KILLER SWITCH (D-E, 28)
   Newly attached for cutting off noise signals. Used in particular adjustments. Close this switch when step states “Place a ground to MOD CON TP-4”.

5. RESONANCE SWITCH (M, 33)
   To emphasize regeneration to the point of oscillation. Used for factory adjustment only.

6. LFO DELAY CONTROL (R, 33)
   From TR25 and TR26 to single paired-transistor TR25 to have U and L delay times synchronize with each other.

7. LFO RATE (V, 33)
   From TR11 and TR12 to single paired-transistor TR11. To minimize speed difference between U and L LFOs.

8. VCO LEVEL (J, 33-34)
   Apply a ground to pin 5 of IC2 through R21, previously —15V. Change resistors values in this section
   To set VCO-1 and VCO-2 audio levels to an equal amount when SOURCE MIX is set at 12 o'clock position.
   To have the same volume changes in VCO-1 and VCO-2 sounds, that is, the change in volume of VCO-1 when SOURCE MIX is being rotated toward VCO-1 is the same as that of VCO-2 when S.M. being toward VCO2.

9. VCA MOD (O, 38-39)
   Add C97 across pins 1 and 2 of IC13
   To eliminate click noises at positive or negative going transient.

10. Add TP-8 (O, 36-37)
    For factory adjustment only.

11. IC49, RAM 2101 and 5101
    SN 202210-UP
    Often, RAM 2101 is substituted by 5101 upon manufacturing or shipping replacement because of procurement problem.
    RAMs of these models have different characteristics in timing response.
    To make both RAMs compatible, factory modification on CPU board started with above Serial number. (See p.38 for detail.)

NOTE:
Beside suffix (A, B, etc.), the PCBs occasionally bear marks “o” above its code number to show the edition, such as “o” for 8th edition.
CHANGES, MODIFICATIONS, ADDITIONS
IN INVOLVED IN IMPLEMENTING DCB
(Digital Communication Bus) BOARD
pp. 40-47
CIRCUIT DESCRIPTION

This circuit description applies to the JP-8 with serial numbers 171700 and up where DAC changed from 12- to 14-bit version, and concentrates on compute program which is revised in line with the change.

This description makes reference to pages 6 and 7 "WIDTH" and "KCV" of the Circuit Description of First Edition issued separately.

WIDTH

P. 6 Change title to WIDTH & TUNE

The coverage of the JP-8 keyboard is expandable to 96 keys using footage selector (RANGE SWITCH). In the following, KCV and key designation are defined as below.

KCV (INTERFACE BOARD)

In this mutual arrangement any KCV (VKnx) at a key (Kn) is obtained from the equations:

\[ VK nx = T(TUNE) - W(WIDTH) \times Kn x \]

where, \( W = \frac{1}{12} \) volt

In the following computuning, \( T \) is a reference voltage in calculating steps with most of pitches slightly out of tune.

To bring each note in tune, the program first adds fine tune voltage (bias) ... \( 0.084 \times 30 \) cents = 0.0252V — to \( T \). Then, finds KCVs for every notes by applying equation (2).

Example: \( VKn24 = 8.025(T) - 0.084(84 - 24) = 2.985V \).

When compare this WIDTH with the WIDTH determined by previous 12-bit system, the new system provides more precise resultant because of wider measurement range.

INITIAL TUNING UPON POWER ON

When the power is first turned on for the JP-8, thermally unstable VCO tends to oscillate on frequencies which are greatly deviating from the expected frequency so that computune circuitry will not be able to determine exact pitch error at a time. If a program encounters such a VCO, the program causes measurement for that VCO but retains the data, then proceeds to the next VCO. After all the VCOs have been measured, the program resumes operation from the first VCO, depending on the previous data. However, the process is repeated only two times per oscillator, regardless of the frequency deviation. Properly functioning VCOs will be brought into tolerance at the second time.

Upon power on for the JP-8, compute program starts frequency measurements at two points with MOD.A first, then MOD.B.

KCV (INTERFACE BOARD)

Each KCV data is represented in 14-bit format and is divided into two pieces—MS (most significant) 8-bit is latched by IC15 followed by LS 6-bit into IC13. DAC output has a range of 0-10V against 14 bits, thus resolution is \( 10V \div 2^{14} \) = 0.6mV, nearly equals 0.7 cents in pitch.

Substituting 0.084 for \( W \) in equation (2) above would provide the VCO with KCVs for every key, and the VCO will oscillate in 1V/oct steps with most of pitches slightly out of tune.

When the power is first turned on for the JP-8, thermally unstable VCO tends to oscillate on frequencies which are greatly deviating from the expected frequency so that computune circuitry will not be able to determine exact pitch error at a time. If a program encounters such a VCO, the program causes measurement for that VCO but retains the data, then proceeds to the next VCO. After all the VCOs have been measured, the program resumes operation from the first VCO, depending on the previous data. However, the process is repeated only two times per oscillator, regardless of the frequency deviation. Properly functioning VCOs will be brought into tolerance at the second time.

Tuning sequence is visually confirmed on flashing LEDs in the PATCH button switches is touched.

However, when one PATCH LED stays on while MANUAL LED is flashing, they are indicating failure in that VCO. The compute program cannot correct such a VCO as is indicated by a PATCH button as below, and does not proceed to the next VCO unless one of function switches is touched.

VCO BEING MEASURED

<table>
<thead>
<tr>
<th>PATCH NO.</th>
<th>MODULE</th>
<th>VCO</th>
<th>MODULE</th>
<th>VCO</th>
</tr>
</thead>
<tbody>
<tr>
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<td>A</td>
<td>1</td>
<td>E</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
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<tr>
<td>5</td>
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<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>D</td>
<td>2</td>
<td>H</td>
<td>2</td>
</tr>
</tbody>
</table>

COMPUTE WITH TUNE BUTTON

When the compute program is triggered manually with TUNE button (after power-on-tune), it runs only once for each VCO since the program already had data on fine tune, and drastic change in VCO frequencies is likely to occur. If the program fails to compensate frequency drift, iterative tapping of "TUNE" will bring VCO closer to correct pitch. Relying on this method is preferable only in an emergency; the cause of out of tune must be eliminated as early as possible.

KCV (INTERFACE BOARD)

P. 7 Lines 9 and 10: Delete

Lines 11-17: Reads as follows.

Each KCV data is represented in 14-bit format and is divided into two pieces—MS (most significant) 8-bit is latched by IC15 followed by LS 6-bit into IC13. DAC output has a range of 0-10V against 14 bits, thus resolution is \( 10V \div 2^{14} \) = 0.6mV, nearly equals 0.7 cents in pitch.

During 1V conversion in IC24, CV for EXT. jack is scaled 1V/oct.

CORRECTION

CIRCUIT DESCRIPTION

P. 11: PUSH SWITCH SCANNING

Push switches (function switches with LED) are read every approximately 25ms (not 1ms). See timing chart on page 3 of the Circuit Description. LEDs are lit every 1ms when INT signal is applied from IC25 which in turn is timed by the signal generated at pin 17 of IC40. Failure of INT signal causes no LED driving signal, but has no relation to the switch reading performance.
DIAGNOSTIC PROGRAM IN PROM D

On the CPU board (of JP-8 furnished with the OC-8 or DCS board) located is IC33 (3.3D or 3.4D) which contains not only digital communication program, but also diagnostic program. The program, when executed in the TEST mode, simplifies testing and fault isolation of some of the ICs and their associated circuits listing to the right. For this program to run, the remaining PROMs (IC34-IC36) of CPU board must be of 3.2 version.

PRECAUTIONS

Allow plenty of time for warm-up (approx. 30 minutes).
If the CPU, PROMs or other circuits fail to perform their basic functions, the program will not start.

STEPS

1. Turn the JP-8 OFF.
2. To put the JP-8 into the TEST mode, either:
   a) Turn the power ON while pressing PATCH NUMBER buttons 1 and 3.
   or
   b) Set SI-1 and SI-2 of the Interface board to TEST, then turn the power ON.

The test program is executed in the order listed and is stopped wherever it encounters a defective IC (or a problem pertaining to a particular IC), and displays the suspected IC number in the window.
To resume the program, press any touch button. (For example, MANUAL.)

At the end of program, the window displays both the PROM D version and the DAC's bit format, for example:

| 33 12 | 3.3D, 12-bit DAC |
| 34 14 | 3.4D, 14-bit DAC |

NOTES FOR TABLE

1. 3.3D doesn't check IC5 and IC6.
2. Because of misprogramming, 3.3D will display these IC numbers in reverse order. If displayed, read: IC49 as IC15, and IC19 as IC20.
3. Output from Module A VCO-1 is applied to the DAC Check. Consequently, if this VCO fails, all the remaining tests will not be performed.
4. IC13 and IC15 on the 12-bit interface board are inversely numbered.
   - IC13 is IC15, and IC15 as IC13.
5. If the 13-bit line malfunctions in the 14-bit D/A, the CPU concludes that the D/A is 12-bit, and skips the 13th and 14th bits.

In the below, SN refers to Serial Number of OP-8.

- For serial numbers up to and including SN220269, the OP-8 was provided with Flat Cable H146 for connecting the OP-8 to the JP-8.
- Effective from serial number SN230270, the OP-8 unit can be connected to the JP-8 through the Flat Cable H146 provided with the OC-8 unit, or to the JUNO-60 through the DCB Cable H165 provided with the OP-8 unit.
- Roland provides not only DCB Cable H165 but also DCB Cable H172 for interconnecting JP-8 or JUNO-60 as shown here.

- DCB Cable H172 is uni-directional, with the signal-flow direction shown by the arrow on the connector.
  When connecting two JUNO-60 or JP-8 units, be sure to connect the cable so that the arrow points away from the JUNO-60 or JP-8 unit to be played, and towards the JUNO-60 or JP-8 unit to be controlled.
  Also, when controlling the JUNO-60 with the OP-8, DCB Cable H172 can be used to connect the OP-8 to the JUNO-60.
  Be sure to connect the cable so that the arrow points away from the OP-8 and towards the JUNO-60. Otherwise, the JUNO-60 may operate incorrectly.
  On the other hand, DCB Cable H165 is a bi-directional cable in which sent from the TX-terminal on a unit returns to the RX-terminal on the unit, causing regeneration.
APPENDIX

PCB EDITION

Dot and circle above PCB code are indicative of edition; "e" stands for 1, and "o" for 5. Example: o = 6th edition.

Illustrated on pp. 48-50 is information on MODULE and MODULE CONTROLLER Boards mounted on the JP-8 models with serial numbers up to 090599. For circuit diagram, refer to p.11 or p.12 although some small discrepancies may exist.

CAUTION ON REPLACEMENT OF PCBs IN THIS SECTION

Although terminal for terminal compatible, when mix used, new and old PCBs process signals in slightly different way, reproducing voices that are distinguishable from each other. Therefore, when replacing MODULE or MOD CON board in this section, use a set of PCBs of the same edition group as described below.

NOTE: Replacement of MODULE board can be made independently of MOD CON board, and vice versa.

MODULE CONTROLLER BOARD

<table>
<thead>
<tr>
<th>Part</th>
<th>SN</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>up to 2B</td>
</tr>
<tr>
<td>C</td>
<td>3A-5B</td>
</tr>
<tr>
<td>C</td>
<td>up to 1B</td>
</tr>
<tr>
<td>D</td>
<td>3A-5B</td>
</tr>
<tr>
<td>J</td>
<td>up to 2B</td>
</tr>
<tr>
<td>J-C</td>
<td>up to 2B</td>
</tr>
<tr>
<td>J</td>
<td>5A-up</td>
</tr>
<tr>
<td>R</td>
<td>up to 2B</td>
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<tr>
<td>D</td>
<td>2x-C</td>
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<td>R</td>
<td>5A-up</td>
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<td>R</td>
<td>3A-5B</td>
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<td>R</td>
<td>3A-5B</td>
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<tr>
<td>R</td>
<td>3A-5B</td>
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<tr>
<td>M</td>
<td>4A-5B</td>
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<tr>
<td>J-C</td>
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<td>J-C</td>
<td>4A-5B</td>
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<tr>
<td>M</td>
<td>4A-5B</td>
</tr>
<tr>
<td>M</td>
<td>3A-5B</td>
</tr>
</tbody>
</table>

ABBREVIATIONS

C-pattern cut Di-diode R-resistor J-jumper M-mylar cap

Listing below are descriptions of surface mounting, jumper wire, and conductive foil cut made on the MOD COM boards up to the abovementioned serial numbers, shown on the next page.

Table:

<table>
<thead>
<tr>
<th>No.</th>
<th>Part</th>
<th>SN</th>
<th>No.</th>
<th>Part</th>
<th>SN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C</td>
<td>up to 2B</td>
<td>10</td>
<td>R</td>
<td>5A-up</td>
</tr>
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<td>C</td>
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<td>11</td>
<td>R</td>
<td>3A-5B</td>
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<tr>
<td>3</td>
<td>C</td>
<td>up to 1B</td>
<td>12</td>
<td>D</td>
<td>2x-C</td>
</tr>
<tr>
<td>4</td>
<td>D</td>
<td>3A-5B</td>
<td>13</td>
<td>M</td>
<td>4A-5B</td>
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<td>R</td>
<td>up to 2B</td>
<td>14</td>
<td>M-C</td>
<td>2A-up</td>
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<tr>
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<td>J</td>
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<td>15</td>
<td>C</td>
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<td>M</td>
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<td>9</td>
<td>R</td>
<td>up to 2B</td>
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### PARTS LIST CHANGE

#### INTERFACE BOARD

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<thead>
<tr>
<th>SERIAL NO.</th>
<th>PART</th>
<th>FROM</th>
<th>TO</th>
<th>PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN 171700</td>
<td>PCB</td>
<td>OPH122</td>
<td>OPH122A</td>
<td>149H122A</td>
</tr>
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<td></td>
<td>D/A</td>
<td>062H268</td>
<td>062H268A</td>
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</tr>
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<td></td>
<td>Converter (IC14)</td>
<td>Latches</td>
<td>Interface Board</td>
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<td>Am6012</td>
<td>ITS80141</td>
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<td></td>
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<td>LS273</td>
<td>TC40H1273 (IC15, CMOS)</td>
<td>15169507</td>
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<td>LS175</td>
<td>TC40H174 (IC13, CMOS)</td>
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<td>LS175</td>
<td>TC40H175 (IC11, CMOS)</td>
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<td></td>
<td></td>
<td>IC25, IC26</td>
<td>HD40156 (CMOS)</td>
<td>151691340</td>
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<td></td>
<td></td>
<td>IC22</td>
<td>TC4001 (Hitachi only)</td>
<td>15169101T</td>
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<td></td>
<td>IC9</td>
<td>LS273</td>
<td>15169105T</td>
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<td>SN 212330</td>
<td>Latches</td>
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<td>IC9</td>
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**CPU BOARD**

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<th>TO</th>
<th>PART NO.</th>
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</thead>
<tbody>
<tr>
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<td>PCB</td>
<td>µPD2716 (version 1.0)</td>
<td>µPD2716-JP8-A (IC36)</td>
<td>15179609 (version 3.x)</td>
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<td>µPD2716-JP8-B (IC35)</td>
<td>µPD2716-JP8-C (IC34)</td>
<td>15179610 (version 3.x)</td>
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<td>15179611 (version 3.x)</td>
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**MODULE CONTROLLER BOARD**

<table>
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<th>PART</th>
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<td>062H269A</td>
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<td></td>
<td>TL082</td>
<td>BA626A</td>
<td>15229802</td>
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<td></td>
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<td>Ladder Resistor</td>
<td>Discrete</td>
<td>R60161B (RA6)</td>
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<tr>
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<td>TRs, 11, 12, 25</td>
<td>2SA1015</td>
<td>15119108</td>
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<td>TR26</td>
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<td></td>
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<td>Switches</td>
<td>SSB212 (Sw 1, 2)</td>
<td>13159123</td>
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<tr>
<td>SN 202210</td>
<td>IC49 RAM</td>
<td>2101 only</td>
<td>2101 or 5101</td>
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**PANEL BOARD F**

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<td>SN 242750</td>
<td>LED (display)</td>
<td>LN526RA</td>
<td>LN5260A</td>
<td>15029409</td>
</tr>
</tbody>
</table>

**PANEL BOARD E**

<table>
<thead>
<tr>
<th>SERIAL NO.</th>
<th>PART</th>
<th>FROM</th>
<th>TO</th>
<th>PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN 272850</td>
<td>Switches (LEDs)</td>
<td>KHC11901 (AR34325S)</td>
<td>KHC11026 (SEL22105)</td>
<td>13169610</td>
</tr>
</tbody>
</table>

In order to expedite delivery of products or because of procurent problem, the factory is occasionally forced to make minor substitution of ICs. Such substitutions will work satisfactorily and compatible with the initial IC unless otherwise noted in related sections (circuit diagram, parts list, etc.).

**PANEL BOARD G**

<table>
<thead>
<tr>
<th>SERIAL NO.</th>
<th>PART</th>
<th>FROM</th>
<th>TO</th>
<th>PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN 282880-UP JP-8 WITH DCB BOARD</td>
<td>PART NAME</td>
<td>FROM</td>
<td>TO</td>
<td>PART NO.</td>
</tr>
<tr>
<td>Top Panel</td>
<td>Chassis (Jack)</td>
<td>Panel H78B</td>
<td>Chassis H116</td>
<td>149H220 (pcb 052H380B)</td>
</tr>
<tr>
<td>Holder (rear)</td>
<td>Panel H116A</td>
<td>Holder H184</td>
<td>064H184</td>
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</tbody>
</table>

**DCB BOARD**

<table>
<thead>
<tr>
<th>PART</th>
<th>FROM</th>
<th>TO</th>
<th>PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Ass'y</td>
<td>OPH220</td>
<td>149H220 (pcb 052H380B)</td>
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<tr>
<td>Holder</td>
<td>H185</td>
<td>064H185</td>
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<tr>
<td>IC1</td>
<td>74LS21</td>
<td>15179112</td>
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<tr>
<td>IC3</td>
<td>µPD8251AC</td>
<td>053H213</td>
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<tr>
<td>Flat Cable</td>
<td>Flat Cable H126 (INTERFACE-CPU)</td>
<td>15179151</td>
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<tr>
<td>DCC Connector</td>
<td>Holder H153</td>
<td>064H153</td>
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<tr>
<td>Slide Switch</td>
<td>SS8-022-12RN</td>
<td>13159118</td>
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**CPU BOARD**

<table>
<thead>
<tr>
<th>PART</th>
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</tr>
</thead>
<tbody>
<tr>
<td>IC33</td>
<td>µPD2718-JP8-D</td>
<td>15179612 (version 3.4)</td>
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</tbody>
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